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Engineering Notes E-114

Page 1 of 8

D-15

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SUBJECT: CHARACTERISTICS OF STANDARD FLIP-FLOP, BASIC CIRCUIT F-F1.
To: 6345 Engineers, Sylvania
From: John M. Hunt
Date: May 21, 1948

SUMMARY

This report outlines the results of tests conducted to determine the operating characteristics and performance specifications of Basic Circuit F-F 1, Drawing B-31559, and has been written to provide quantitative data to expedite design and testing of circuits incorporating the basic flip-flop as a component.

A description of several early type flip-flops, as well as the preliminary design of the existing basic flip-flop, is included in Report E-113. Since Report E-113 was written (March 19, 1947) several circuit changes have been made which appreciably alter the performance of the flip-flop circuit.

D. C. Flip-Flop Operation

Because of the fact that the cross-feed resistors, which couple the plates of the flip-flop to the opposite grids, are direct coupled (i. e., no blocking capacitors are used to isolate the d.c. components of the feedback signals) performance of the basic flip-flop is independent of frequency from zero to the maximum usable frequency of at least 5 megacycles. The upper frequency limit is determined by switching time, which is primarily controlled by the time constant of the R-C combination of output-circuit capacitance and plate-load resistance. Operating voltages and currents, and component dissipation, are therefore independent of switching frequency (neglecting the very slight effects of circuit capacitances and inductances at high frequencies). Consequently, determination of these operating characteristics with the flip-flop in the steady-state condition is possible.

Although 1 percent tolerance resistors have been specified for the flip-flop of W/I, variations of 6AG7 tube characteristics and supply voltages result in appreciable changes in circuit currents, voltages, and dissipation. Using a pair of 6AG7 tubes having characteristics which approach the average of a number of production tubes tested, and maintaining supply voltages at the design values of 120 volts for screen supply and 150

volts plate supply, the following data were obtained:

(All indicated voltages were measured with respect to ground and are actual circuit voltages with no error attributable to voltmeter loading of the circuit.)

<u>Voltages and Currents</u>	<u>On Tube</u>	<u>Off Tube</u>
Plate Voltage	76.5 v	108.5 v
Cathode Voltage	31 v	31 v
Screen Voltage	118 v	120 v
Control Grid Voltage	31 v	21.5 v
Plate Current	27 ma	0 ma
Screen Current	9 ma	0 ma
Control Grid Current	0.5 ma	0 ma
Total Current from +150 v supply		53.5 ma
Total Current from +120 v supply		9.0 ma

<u>Tube Dissipations</u>	<u>Rated Maximum</u>	<u>Actual Dissipation</u>
Plate Dissipation	9 watts	1.23 watts
Screen Dissipation	1.5 watts	0.79 watts
Control Grid Dissipation		Negligible

<u>Resistor Dissipations</u>	<u>Resistor Rating</u>	<u>Actual Dissipation</u>
1500 ohm Plate Load Resistor	8 watts	2.31 watts
5000 ohm Feed-Back Resistor	8 watts	1.56 watts
2000 ohm Grid Resistor	8 watts	0.48 watts
820 ohm Cathode Resistor	2 watts	1.13 watts
220 ohm Plate Decoupler	2 watts	0.64 watts
220 ohm Screen Decoupler	1 watt	0.02 watts

Note that all dissipations, with the exception of 6AG7 screen grid and 820-ohm cathode resistor, are less than one-half of the corresponding rated maximums. The 6AG7 screen dissipation is 53 percent of rated maximum and 820 ohm cathode-resistor dissipation is 57 percent of rated maximum.

Pulsed Operation of Flip-Flop

From the preceding data the plate-voltage change from on to off for d.c. operation is observed to be 32 volts. For pulsed operation with 120 volt screen supply and 150 volt plate supply the plate voltage excursion during switching is also 32 volts at all frequencies up to the maximum usable switching frequency of approximately 5 megacycles. A ten-volt reduction on

both screen and plate supply voltages reduces the plate voltage swing during switching to 29 volts, while a 10 volt increase in plate and screen supply voltages increases the output voltage to 36 volts. The flip-flop circuit is stable with considerably greater variations in plate and screen supply voltages but operation of WWI under such conditions is not anticipated.

The magnitude of the trigger pulse does not affect output voltage swing, nor does output circuit loading by gate tubes or indicator circuits. However, capacitance shunted across the plate load does increase the rise time of the circuit during switching (see Figures 1 to 12).

Variations of screen and plate supply voltages affect the sensitivity of the flip-flop to trigger pulses, but the change in minimum pulse amplitude required to trigger the flip-flop is negligible for ± 10 volts variation in supply voltages. With 150 volt plate supply voltage and 120 volt screen supply voltage a 0.1 microsecond half-sine wave pulse of approximately six volts amplitude will trigger the flip-flop, pulse sensitivity being approximately the same for pulses applied either to control grid or to cathodes, positive pulses being applied to the cathode and negative pulse to the grid, respectively.

Output Wave Shapes

A Model 5 synchroscope was used to determine the output voltage wave shapes of the flip-flop. The upper vertical deflection plate was connected to the plate of one of the flip-flop tubes through a 120 micromicrofarad mica capacitor, the cathode-ray tube deflection plate being returned to ground through a 0.82 megohm resistor. The capacitance of the deflection circuits and test lead was approximately 15 micromicrofarads. The synchroscope trace was photographed, the horizontal sweep speed having been adjusted to cause two large divisions (20 small divisions) of the coordinate grid-work to correspond to exactly one microsecond. Each small division vertically corresponds approximately to six volts input signal voltage to the deflection plate. Figures 1 to 12 are typical output voltage wave oscillograms under various pulse and output capacitance loading conditions.

Figures 1 to 6, Drawing A-32265, and Figures 7 to 12, Drawing A-32266, are photographs of the output wave shapes of a flip-flop with 15 volt paired restorer pulses, spaced one microsecond at a repetition rate of 10 kilocycles driving the cathodes of the flip-flops. In each of the twelve photographs an additional pulse, timed to occur during the one microsecond interval between the restorer pulses, is applied to the flip-flop each time the synchroscope trace is triggered. As a result the flip-flop tube to which the synchroscope is connected is caused to switch from Off to ON with each alternate trace of the synchroscope; the effect of this reversal, combined with the restorer action (which occurs at the extreme edges of the photograph) is to produce the double trace observed in Figures 1 to 12. It

should be understood that only one trace appears with each sweep, the two traces appearing alternately at a frequency corresponding to the trigger pulse repetition frequency of 10 kilocycles and that the plate voltage of only one of the flip-flop tubes is being observed.

In Figures 1 to 6 negative trigger pulses were fed to the grid circuit of the flip-flop; in Figures 7 through 12 positive trigger pulses were applied to the cathode. The magnitude of the pulses is indicated under each photograph. Figures 1 to 3 and 7 to 9 indicate output voltage with no shunt capacitances other than the standard flip-flop circuit wiring, an output coupling circuit CC-1 and indicator circuit IND-1. No gate tube was connected to the flip-flop as the synchroscope deflection-input capacitance approximately is equivalent to the typical load capacitance which would be encountered in WWI applications of the basic flip-flop. In Figures 4 to 6 and 10 to 12 an additional 20 micromicrofarad mica capacitor has been shunted from each flip-flop plate to ground to simulate an unusually heavily loaded flip-flop. It is not anticipated that appreciable conductance will be shunted across the flip-flop plate circuit by the type of loads used in WWI, although the low output impedance of the flip-flop (of the order of 1500 ohms) permits some output-load shunt conductance without serious reduction in flip-flop output voltage or reliability of performance.

Note that the trigger pulses, particularly if of considerable magnitude, appear as distortion in the output wave shape, cathode trigger pulses appearing as positive pulses superimposed on the plate voltage and grid pulses appearing as negative pulses on the plate wave forms.

Switching time can be estimated from the photographs without difficulty. Resolution time (i. e., the minimum time separation between two adjacent pulses which will permit the flip-flop to respond to both the individual pulses) cannot be determined from the photographs in this report but has been observed to be of the order of 0.15 microseconds, although this figure is only a rough approximation as pulse shape and magnitude appreciably affect resolution time.

The output voltage on all of the photographs is approximately 32 volts. Because of the 100-microsecond time constant of the R-C coupling circuit which isolates the d.c. component of flip-flop plate voltage from the vertical deflection plates, the difference in voltage between the two successive (upper and lower) traces immediately ahead of the first restorer pulse is less than 32 volts, as at this point the upper trace has been falling and the lower trace has been rising for 9 microseconds because of charging of the 120 micromicrofarad coupling capacitor in the synchroscope deflection circuit. At low values of restorer-pulse repetition rate or low synchroscope coupling circuit time constant the effect of synchroscope coupling time constant is quite pronounced, the two traces to the left of the first restorer pulse approaching one another closely and separating a corresponding amount to the right of the first restorer pulse. Unless a synchroscope coupling time constant of less than 50 microseconds is used the difference between the voltages indicated by one of the two traces immediately before and immediately after switching, is very nearly equal to the actual flip-flop voltage swing during switching.

Starting of Flip-Flop

Because of the clamping circuit connected to the flip-flop plate circuit, difficulty may be experienced in causing the flip-flop to start (i. e. to respond to restorer pulses when the flip-flop has been at d. c. equilibrium for one second or more). The reason for this difficulty is that the 0.01 microfarad coupling capacitor connected to the conducting flip-flop tube plate is charged to a voltage equal to the plate-to-ground voltage of the conducting flip-flop tube when the flip-flop has been at d.c. equilibrium for one second or more. Attempts to trigger the flip-flop are unsuccessful unless the On tube of the flip-flop is driven to cut-off for a period of time long enough for this 0.01 microfarad capacitor to charge through the forward resistance of the IN34 clamp rectifier and effective generator impedance of the flip-flop output circuit to a voltage sufficiently high to cause the Off tube, because of positive voltage feed back through the cross feed resistors from the opposite plate circuit, to begin to conduct. After the flip-flop upsets, subsequent response to trigger pulses is normal (if the pulse prf is not too low).

Because of the relatively low discharge time constant of the coupling circuit it is not necessary that the capacitor be charged by a single pulse, a prolonged sequence of pulses permitting incremental increases in capacitor voltage until the plate voltage reaches a value sufficiently high to upset the flip-flop. However, as the voltage across the capacitor increases, the rate of loss of charge between pulses increases and it is therefore possible for the capacitor voltage to reach an equilibrium value for a given recurrent trigger pulse, which is not sufficiently high to upset the flip-flop. The result is that the flip-flop cannot be started unless the pulse repetition rate is increased, pulse magnitude is increased, or some expedient such as momentarily removing the flip-flop screen voltage is utilized.

For a given pulse width and voltage the minimum prf necessary for flip-flop self starting is determined by the ratio of discharge to charge time constants of the coupling circuit. This ratio is determined primarily by the back resistance of the IN34 clamp rectifier, the charge time constant not being appreciably affected by the low forward resistance of the IN34 except at very low voltages. The back-to-front resistance ratio of the IN34 increases greatly with increased crystal voltage - for this reason an operating flip-flop is not appreciably loaded by the coupling circuit as the crystal back-resistance increases during flip-flop operation to a value which reduces clamp circuit discharge between restorer cycles to a negligible amount.

A shunt resistance of 0.27 megohms across a clamp circuit IN34 having very high back resistance (considerably greater than one megohm at 20 volts when tested on a WW standard IN34 tester) permitted reliable

self-starting with application of 16 microsecond standard 15 volt paired restorer pulses to the flip-flop cathodes. An 0.18 megohm shunt caused unreliable starting under similar circumstances, while a 0.1 megohm shunt resistor prevented starting with 10 microsecond restorers.

The extreme variation of IN34 resistance with applied voltage precludes the possibility of accurately specifying a minimum back resistance (measured at a fixed test voltage) which will assure reliable flip-flop self starting at all times. It is believed that IN34's having the highest available back resistance within reasonable commercial limitations should be used for flip-flop output coupling clamp crystals if self starting is essential. In the event that it is not practicable to use circuit constants such that self starting is possible, the flip-flops can be easily started by momentary removal of screen voltage; the fact that such a circuit requires external action to initiate operation is not in reality a serious disadvantage since it is obvious that self re-starting of an ostensibly operative flip-flop which has failed to operate for a short period will very probably cause more trouble than complete failure of the flip-flop.

Self-starting ability is not appreciably improved by reduction of the capacitance of the output coupling capacitor unless the capacitance is reduced to an unreasonably low value. It is necessary that a moderately large coupling capacitor be used to maintain a high coupling circuit time constant, otherwise restorer repetition rate must be unduly increased.

Sensitivity to Power-Supply Fluctuations:

Rapid changes of screen or plate supply voltage, such as might be caused by the operation of other pulsed circuits on a common power supply with the flip-flop, can result in triggering of the flip-flop. To determine the approximate sensitivity of the flip-flop to triggering by such unwanted pulses a circuit was constructed wherein an approximately rectangular pulse of 4 microsecond duration and having a 0.2 microsecond rise time could be inserted in series with the plate or screen supply lines of the flip-flop.

Both positive and negative pulses were applied to the screen supply line, to the plate supply line, and to the screen of one of the flip-floptubes, the other screen being operated at 120 volts without an interference pulse. Figures 13 to 18, Drawings SA-38417 and SA-38418, indicate the appearance of the supply-line pulse and the corresponding pulse at the output or flip-flop side of the 220-ohm 0.01 microfarad decoupling filter in the corresponding supply lead. Figures 13 and 14 represent the pulse applied to both screens. Figures 15 and 16 represent the pulse applied to one screen only, while application of pulses to the plate supply line is indicated in Figures 17 and 18.

Figures 14 and 16 (positive pulses applied to both screens and to one screen only) indicate the maximum pulse available from the pulse generator, a value which was insufficient to trigger the flip-flop (the existing flip-flop is quite insensitive to increase in screen supply voltage). The remaining figures of the group indicate the minimum supply pulse necessary to trigger the flip-flop. It is interesting to note that the flip-flop is relatively insensitive to such power supply disturbances, and that the decoupling circuit does not appear to be particularly effective in removing comparatively long duration (4 microsecond) pulses on the supply voltages.

Marginal Testing by Lowering Screen Voltages

One of the most promising methods of detecting the presence of marginal flip-flop tubes in the computer is observation of flip-flop performance with one of the tubes operating at reduced screen voltage, weak tubes presumably being less tolerant of reduction in screen voltage than good tubes. Four 6AG7 tubes which had been operated for 1500 hours in a life-test rack were used in a test flip-flop to determine the effectiveness of the proposed marginal tube detection scheme. Because of the performance of these tubes in various flip-flops in the laboratory and because of the length of time these tubes were operated in the life test rack it is believed that they were representative of marginal tubes to be encountered in operation of WWI.

The following table indicates the range of screen voltage variation (on one tube only - the screen of the other tube was maintained at 120 volts during the tests) throughout which the flip-flop is stable.

Flip-Flop Tube Numbers		Range Screen Voltage for Stable Operation	
Left Tube	Right Tube	Left Tube Screen Voltage Varied	Right Tube Screen Voltage Varied
1	2	90 - 170	84 - 175
1	3	86 - 175	85 - 183
1	4	95 - 166	80 - 163
2	3	89 - 186	89 - 190
2	4	95 - 162	80 - 161
3	4	87 - 200	80 - 154

In view of the above information, which is, of course, quite incomplete, it appears that lowering of the screen supply lines individually will provide a reasonably satisfactory check on marginal tubes. It should be realized, however, that with the best available paired 6AG7 flip-flop tubes reduction of one screen to approximately 85 volts results in instability. Hence the method certainly is not foolproof and care must be taken to determine the most realistic value of depressed screen voltages consistent with detection of the maximum number of marginal tubes and the rejection of the minimum number of good tubes.

6345
Engineering Notes E-114

Page 8 of 8

Drawings: A-32265
A-32266
SA-38417
SA-38418

Signed: John M. Hunt
John M. Hunt

Approved: DRB
David Brown

JMH/nds

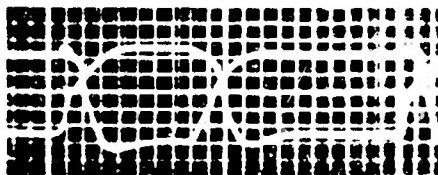


FIGURE 1
15 MMF EXTERNAL
SHUNT CAPACITANCE

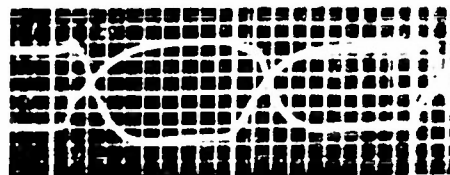


FIGURE 4
35 MMF EXTERNAL
SHUNT CAPACITANCE

7.5 VOLT TRIGGER PULSES
TO FLIP-FLOP GRID

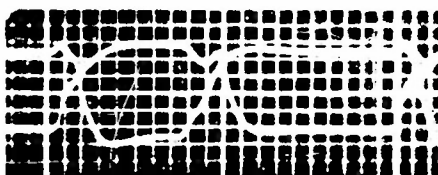


FIGURE 2
15 MMF EXTERNAL
SHUNT CAPACITANCE

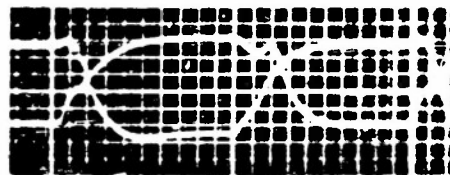


FIGURE 5
35 MMF EXTERNAL
SHUNT CAPACITANCE

15 VOLT TRIGGER PULSES
TO FLIP-FLOP GRID

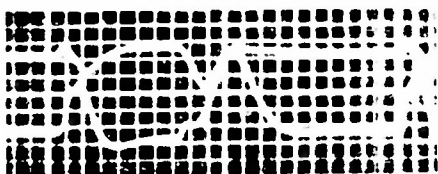


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15 MMF EXTERNAL
SHUNT CAPACITANCE

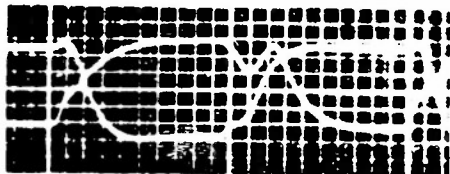


FIGURE 6
35 MMF EXTERNAL
SHUNT CAPACITANCE

30 VOLT TRIGGER PULSES
TO FLIP-FLOP GRID

FLIP-FLOP OUTPUT VOLTAGE WAVE SHAPE
SWEEP SPEED 0.5 MICROSECOND PER INCH

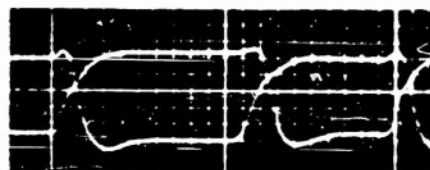


FIGURE 7
15 MMF EXTERNAL
SHUNT CAPACITANCE



FIGURE 10
35 MMF EXTERNAL
SHUNT CAPACITANCE

7.5 VOLT TRIGGER PULSES
TO FLIP-FLOP CATHODE

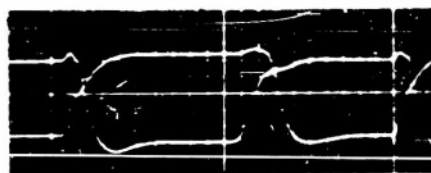


FIGURE 8
15 MMF EXTERNAL
SHUNT CAPACITANCE



FIGURE 11
35 MMF EXTERNAL
SHUNT CAPACITANCE

15 VOLT TRIGGER PULSES
TO FLIP-FLOP CATHODE

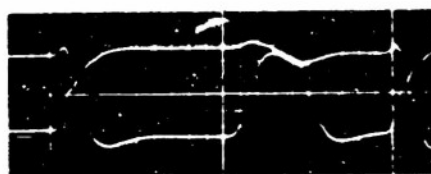


FIGURE 9
15 MMF EXTERNAL
SHUNT CAPACITANCE

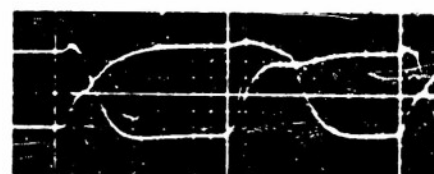
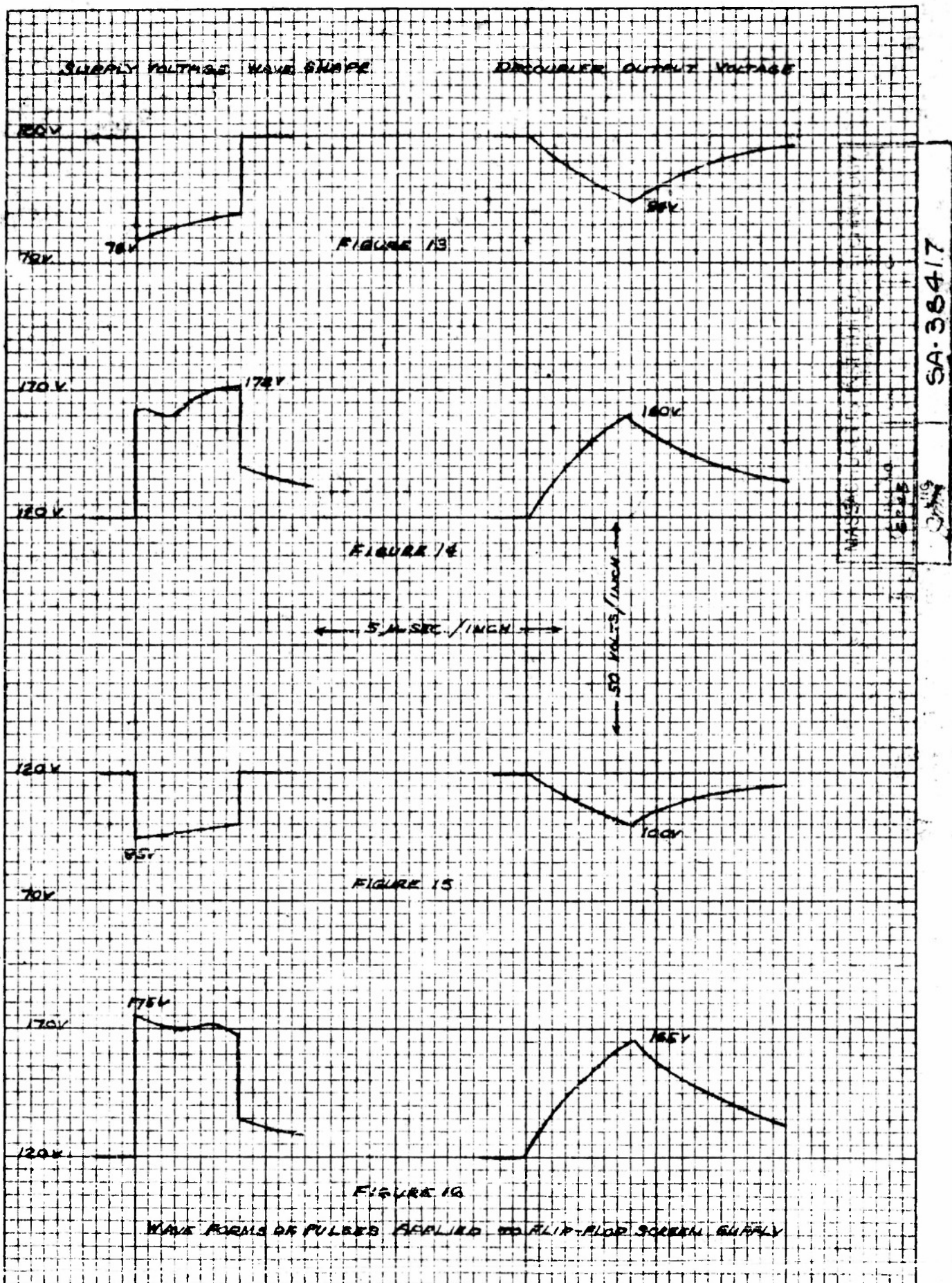
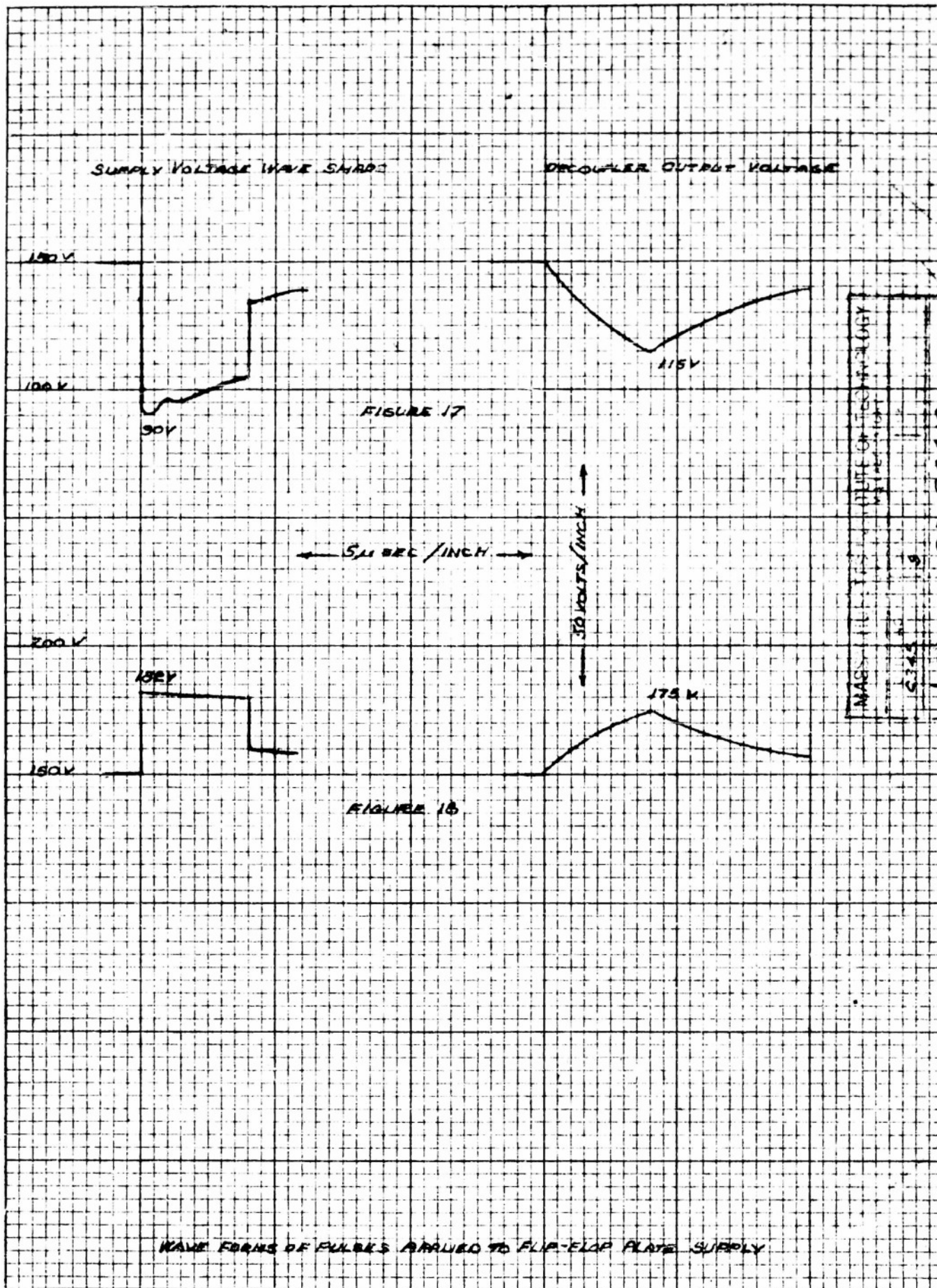


FIGURE 12
35 MMF EXTERNAL
SHUNT CAPACITANCE

30 VOLT TRIGGER PULSES
TO FLIP-FLOP CATHODE

FLIP-FLOP OUTPUT VOLTAGE WAVE SHAPE
SWEEP SPEED 0.5 MICROSECOND PER INCH





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